In the Claims:

Claims 1-17 have been previously canceled. Please cancel claims 27 and 32, and please amend claims 28, 30 and 31, as indicated below.

1.-17. (Canceled)

18. (Previously presented) An isolation structure laterally disposed between a first active region and a second active region of a semiconductor substrate, comprising:

a trench formed within said semiconductor substrate;

a thermally grown oxide layer having a first portion disposed across a bottom of said trench, and second and third portions disposed within said trench laterally adjacent to said first and second active regions;

a deposited oxide disposed within said trench above said first portion and between said second and third portions, said deposited oxide having an upper surface which is approximately coplanar with an upper surface of said semiconductor substrate; and

implanted silicon atoms arranged within regions of said first and second active regions proximate said upper surface of said substrate and laterally adjacent to said second and third portions of said thermally grown oxide, wherein the implanted silicon atoms fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of said trench.

19. (Previously presented) The isolation structure as recited in claim 18, wherein the implanted silicon atoms are arranged within the first and second active regions directly beneath a spacer.

20. (Previously presented) The isolation structure as recited in claim 19, wherein the spacer extends from a sidewall of a masking layer residing over the semiconductor substrate to the lateral perimeter of the trench.

21. (Previously presented) The isolation structure as recited in claim 20, wherein the lateral distance between the sidewall of the masking layer and the trench, over which the spacer extends, is approximately 0.1 micron.

22. (Previously presented) A semiconductor topography, comprising:

a dielectric filled trench arranged within a semiconductor substrate; and

barrier atoms arranged within the semiconductor substrate beneath a spacer that extends above a portion of the semiconductor substrate between the trench and a sidewall surface of a masking layer, wherein the barrier atoms fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of said trench.

23. (Previously presented) The semiconductor topography as recited in claim 22, wherein the spacer is configured laterally between a peripheral of the trench and the sidewall surface of the masking layer.

24. (Previously presented) The semiconductor topography as recited in claim 22, wherein the spacer is made of a different material than the dielectric of the dielectric filled trench.

25. (Previously presented) The semiconductor topography as recited in claim 22, wherein the barrier atoms are selected from the group consisting of nitrogen, argon and germanium, or combinations thereof.

26. (Previously presented) The semiconductor topography as recited in claim 22, wherein the barrier atoms are arranged within an active region of the semiconductor substrate within 0.1 micron of the trench.

27. (Canceled)

28. (Currently amended) ~~The~~ An integrated circuit ~~as recited in claim 27~~, comprising:

a semiconductor substrate having a trench isolation structure formed therein;

active regions within the semiconductor substrate extending to opposing edges of the trench isolation structure; and

implanted silicon and barrier atoms arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure, wherein the implanted silicon and barrier atoms fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure

~~wherein the implanted silicon or barrier atoms arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure comprise both implanted silicon atoms and barrier atoms~~.

29. (Previously presented) The integrated circuit as recited in claim 28, wherein the barrier atoms are selected from the group consisting of nitrogen, argon and germanium, or combinations thereof.

30. (Currently amended) ~~The~~ An integrated circuit ~~as recited in claim 27~~, comprising:

a semiconductor substrate having a trench isolation structure formed therein;

active regions within the semiconductor substrate extending to opposing edges of the trench isolation structure; and

implanted silicon atoms arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure, wherein the implanted silicon atoms fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure

~~wherein only implanted silicon atoms are arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure to fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure~~.

31. (Currently amended) The integrated circuit as recited in claim ~~27~~ 30, wherein only ~~barrier~~ implanted silicon atoms are arranged within the semiconductor substrate at each of the opposing edges of the trench isolation structure to fill vacancies and interstitial sites within the semiconductor substrate resulting from formation of the trench isolation structure.

32. (Canceled)